**The development of the chip for data collection and processing**

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***Summary* —The Article provides the description of the data collection and processing chip. The most important parameters are considered by the 1273ПВ10Тexample.**

***Keywords* —Design, analog circuits, component base.**

**Abstract**

OAO NIIET has developed the chip for the 16 channel 16bit1273ПВ10Т ADC.

1273ПВ10Тchip belongs to the analog process class. Analog preprocessors are applied along with the DSP in the modern aircraft control systems, ground-based diagnostic systems for avionics, on-board data collection and processing systems.

1273ПВ10Тchip is a16 bit CMOS ADC with sequential access interface. It has a signal/noise ratio of 77 database within the frequency band from 0 to 4 kHz. Each channel as a programmable input amplifier with again range from 0 to 38 dB. Conversion frequency can be programmed for four values: 64, 32, 16 or 8 kHz (when the input clock frequency is 16.384MHz). The serial port allows you to use the chip switched in cascade according to standard protocols DSP processors. Communication speed through the serial port is programmable that allows to use the chip with both fast and slow processors DSP.

The block diagram is provided. An internal source forms the power supply. Internal voltage source comes to the output that is used to connect an external capacitor. If this output is used as a reference source, it is mandatory to provide the buffering.

Serial port provides a digital configuration data input and output from the eight internal registers and the output of the transformation results.

This device contains six identical channels of analog data processing.

An integrated amplifier with a programmable gain, which is a switched capacitor circuit, is part the sigma-delta modulator. Output voltage level of the amplifier must not exceed the maximum input level of sigma-delta modulator.

The built-in digital filter performs two important functions. At first, it's the removal of the analog modulator generated quantization noise outside the working frequency band and at second it's a thinning of flow of the high frequency single-bit words to the 15-bit stream of low frequency words. Antialiasing decimation filter is a digital filter with a characteristic in the form of sinc3, which reduces the sampling frequency and increases the resolution from 1 to 15 bits. Z-transform transfer function expressed as a ratio [(1-Z-32) / (1-Z-1)] 3. This guarantees a minimum group delay of 25 ms.

A specific feature of the circuit is a presence of programmable divider of the reference frequency which allows the user to reduce the frequency of an external clock signal. Clock divider allows the user to adjust the value of the clock frequency to the data.

Thinning divider enables the user the flexibility to adjust the value of the ADC sampling device to the desired DSP program.

Input and output datum are transmitted in a multiplex time division multiplexing format(TDM). For the reading data from the chip, each channel has a fixed time interval in which the data is transmitted.

Circuit is designed to support up to eight devices in the cascade when connected to a single serial port. Serial port connection protocol is designed so that the addressing the device is contained in the sets of data transferred device. This allows generating a cascade without any additional hardware costs for the address and control signals. The cascade may be formed in the software and combined modes.

Each channel of the chip can be used as a differential or single-ended input signal, which can be inverted by the input signal generator. The input signal can be connected to the DC level when the DC offset of the input signal is equal to the internal reference voltage level.